

Appln. No.: 10/055,120

Reply to Office action of December 23, 2005

Amendments to the Claims:

Please cancel claims 48, 49 and 51 as shown in the listing of claims below. This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-42 (cancelled)

43. (previously presented) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system comprising:

(a) a set of phase detectors generating phase errors for the set of sampling clock signals;

(b) a set of loop filters coupled to the set of phase detectors, the loop filters receiving the phase errors and generating filtered phase errors;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the set of D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems;

wherein the set of clock signals further comprises a receive clock signal and wherein each of the processing subsystems further comprises a digital section, the digital sections operating in accordance with the received clock signal;

wherein the receive clock signal is related to one of the sampling clock signals.

Claims 44-51 (cancelled)

52. (previously presented) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals, the processing system comprising

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a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system comprising:

- (a) a set of phase detectors generating phase errors for the set of sampling clock signals, wherein each of the phase detectors receives a corresponding slicer error and a corresponding tentative decision from a decoding system;
- (b) a set of loop filters coupled to the set of phase detectors, the loop filters receiving the phase errors and generating filtered phase errors;
- (c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and
- (d) a set of oscillators coupled to the set of D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems.

53. (previously presented) The timing recovery system of claim 52 wherein each of the phase detectors comprises a lattice structure, the lattice structure comprising two delay elements, two multipliers and an adder, the lattice structure generating a pre-cursor phase error by multiplying the corresponding tentative decision by a delayed version of the corresponding slicer error and generating a post-cursor phase error by multiplying the corresponding slicer error by a delayed version of the corresponding tentative decision and combining the pre-cursor and post-cursor phase errors to produce the corresponding phase error.

54. (previously presented) The timing recovery system of claim 53 wherein at least one of the phase detectors further receives an offset input from a control unit and wherein the associated lattice structure combines the pre-cursor, post-cursor phase errors and the offset input to produce the corresponding phase error.

55. (previously presented) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals

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associated with a corresponding plurality of input signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system comprising:

(a) a set of phase detectors generating phase errors for the set of sampling clock signals;

(b) a set of loop filters coupled to the set of phase detectors, the loop filters receiving the phase errors and generating filtered phase errors, wherein at least one of the loop filters comprises a first filter for accumulating a number of consecutive values of one of the phase errors to produce a filtered phase error;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the set of D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems.

56. (previously presented) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system comprising:

(a) a set of phase detectors generating phase errors for the set of sampling clock signals;

(b) a set of loop filters coupled to the set of phase detectors, the loop filters receiving the phase errors and generating filtered phase errors, wherein at least one of the loop filters comprises a first filter for accumulating a number of consecutive values of one of the phase errors to produce a sum value, and a second filter for integrating the sum value to produce an integral value and an adder for combining the sum value and the integral value to produce a filtered phase error;

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(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the set of D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems.

57. (previously presented) The timing recovery system of claim 56 wherein the second filter includes a multiplier for scaling an integrated sum value by a scale factor to produce the integral value.

Claims 58-60 (cancelled)